

Polymorphic Heterogeneous Multi-core Systems

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The objective of this project is to develop the design space exploration technique for a polymorphic heterogeneous multi-core architecture that can be tailored according to the workload by software. The architecture is designed and fabricated as a heterogeneous multi-core system containing multiple identical cores and memory modules and small amount of reconfigurable logic on chip. Post-fabrication, software can configure or compose together primitive on-chip hardware components to create a customized multi-core system that best matches the needs of a specific application. An appropriate software tool chain consisting of compiler and smart design space exploration techniques is required to identify and map an application to the appropriate configuration. The thesis project would involve developing and implementing an efficient design space exploration technique for the architecture.

Relevant Publications:

1. [Shared Reconfigurable Fabric for Multi-Core Customization](#)

Liang Chen, Tulika Mitra

Design Automation Conference (DAC), June 2011

2. [Customized MPSoC Synthesis for Task Sequence](#)

Liang Chen, Nicolas Boichat, Tulika Mitra

IEEE Symposium on Application Specific Processors (SASP), June 2011

Project Schedule:

Month 1: Literature survey and familiarization with toolchain

Month 2: Develop compile time performance estimation technique for loop kernels on reconfigurable fabric with varying loop unrolling and software pipelining

Month 3: Implementation of the compile time estimation technique

Month 4: Develop and implement design space exploration algorithm for multi-core system

Month 5: Develop and implement design space exploration algorithm for multi-core system

Month 6: Report write-up

Profile:

The candidate should have good programming skills and should have a strong background in one or more of the following areas:

- Operating Systems
- Compilers
- Computer Architectures